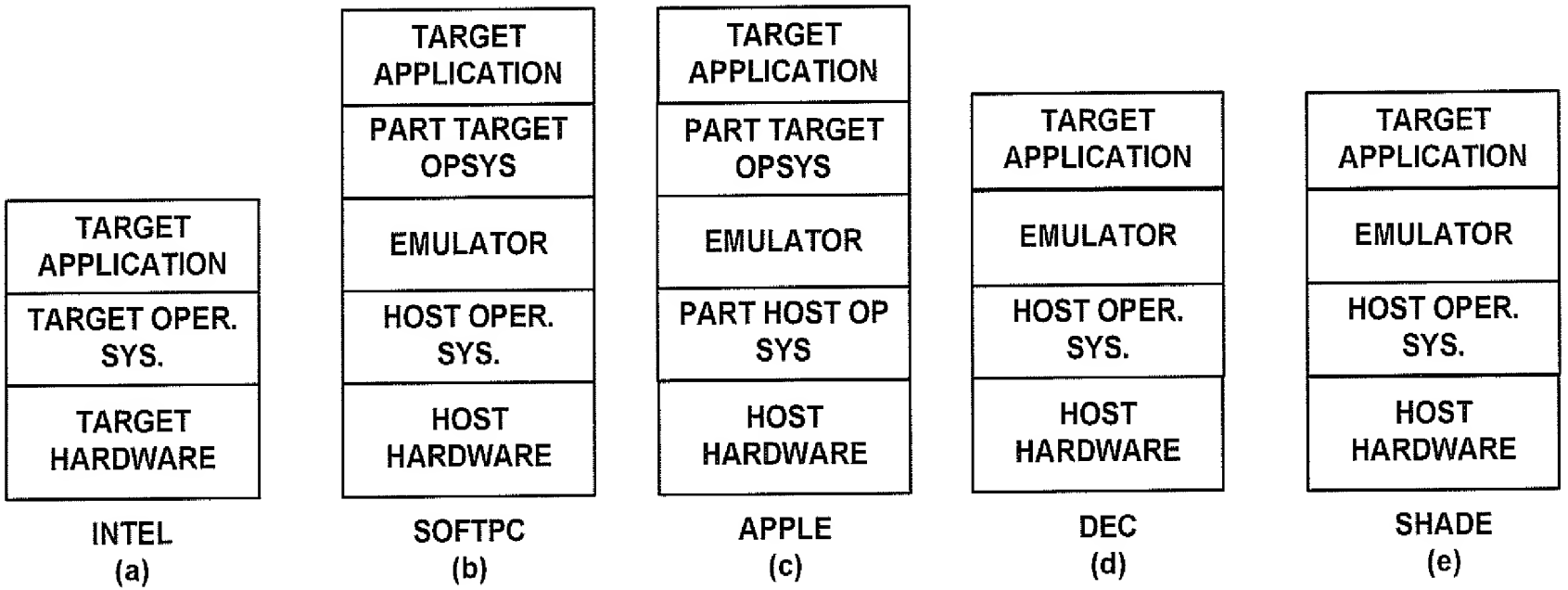
TARGET APPLICATION
TARGET OPER. SYS.
TARGET HARDWARE
INTEL
(a)
TARGET APPLICATION
PART TARGET OPSYS
EMULATOR
HOST OPER. SYS.
HOST HARDWARE
SOFTPC
(b)
TARGET APPLICATION
PART TARGET OPSYS
EMULATOR
PART HOST OP SYS
HOST HARDWARE
APPLE
(c)
TARGET APPLICATION
EMULATOR
HOST OPER. SYS.
HOST HARDWARE
DEC
(d)
TARGET APPLICATION
EMULATOR
HOST OPER. SYS.
HOST HARDWARE
SHADE
(e)

FIGURE 1

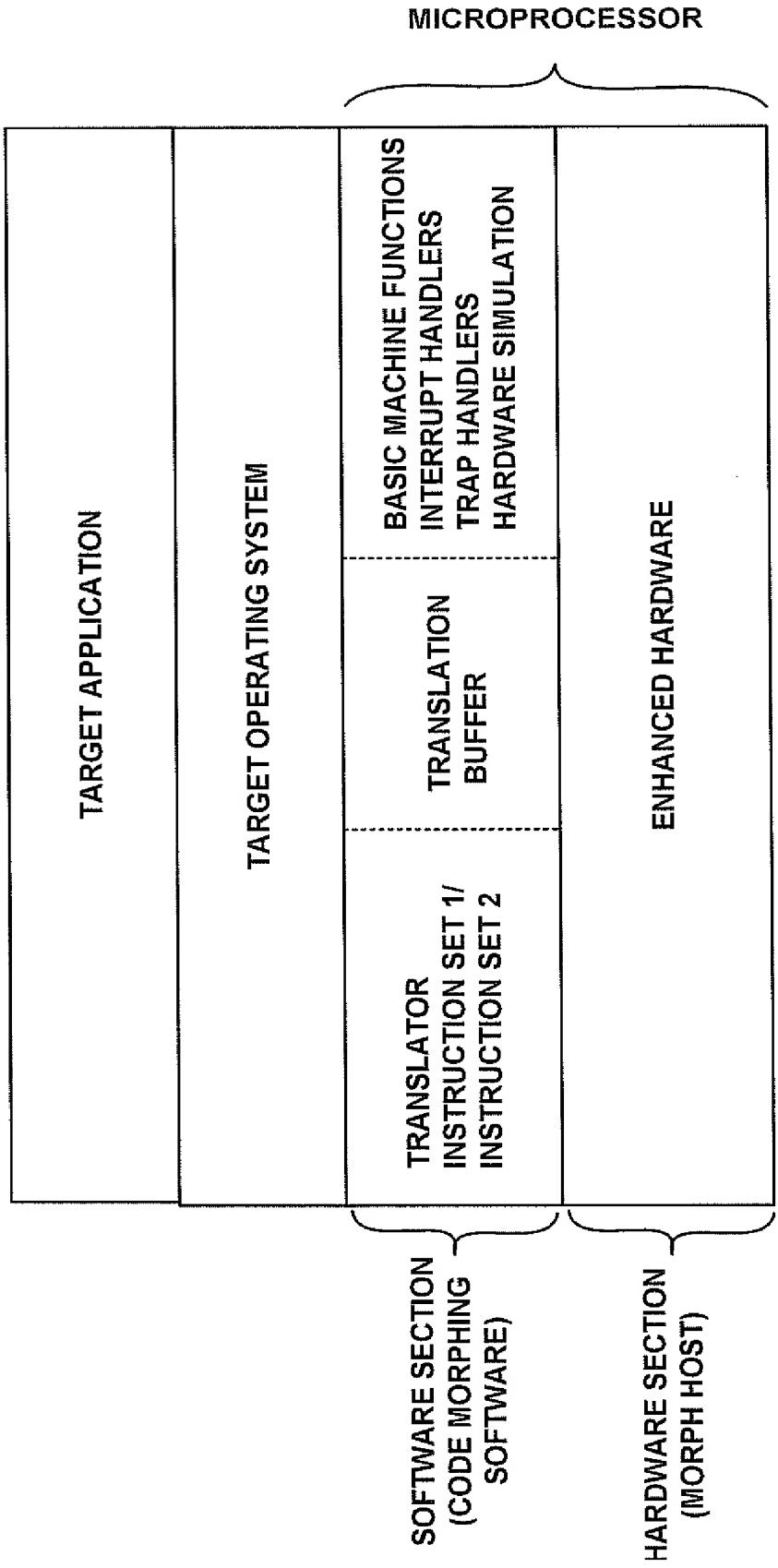
MICROPROCESSOR
TARGET APPLICATION
TARGET OPERATING SYSTEM
BASIC MACHINE FUNCTIONS
INTERRUPT HANDLERS
TRAP HANDLERS
HARDWARE SIMULATION
TRANSLATION BUFFER
TRANSLATOR INSTRUCTION SET 1/ INSTRUCTION SET 2
ENHANCED HARDWARE
SOFTWARE SECTION (CODE MORPHING SOFTWARE)
HARDWARE SECTION (MORPH HOST)

FIGURE 2

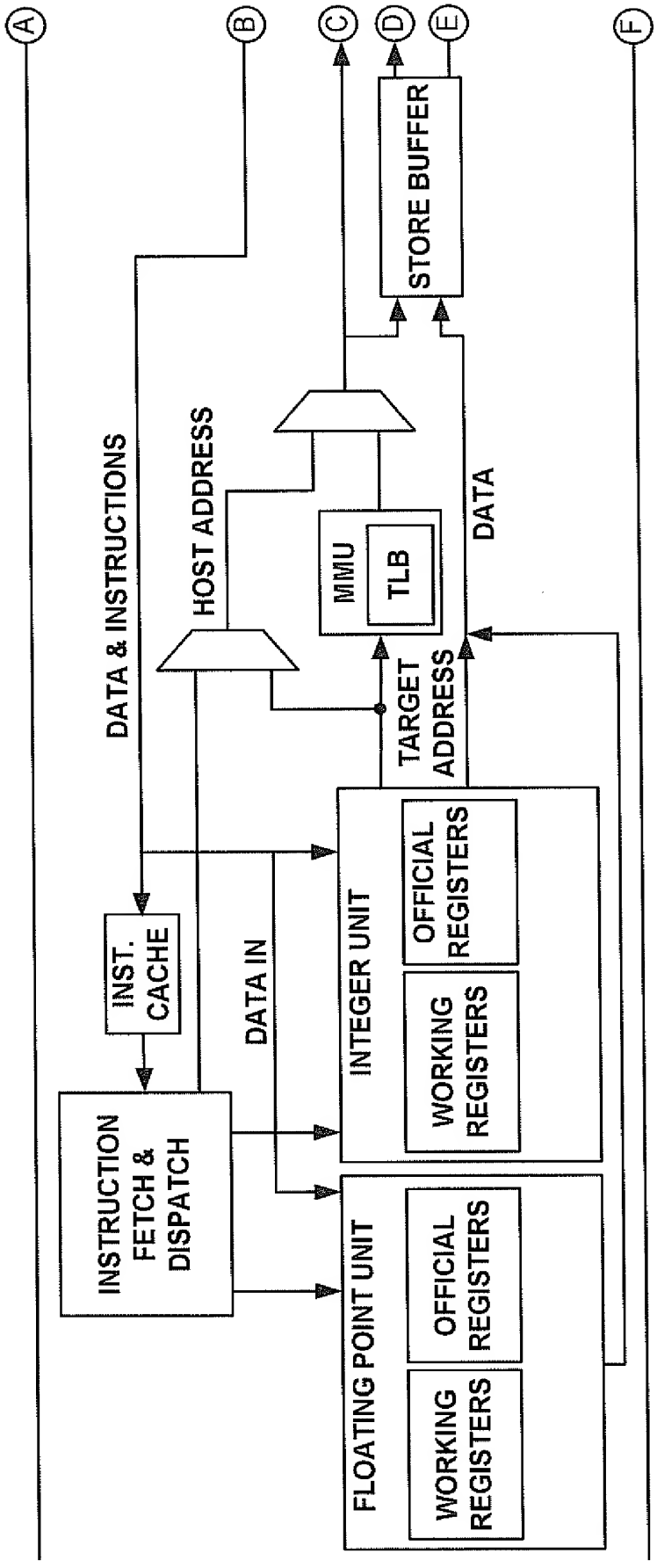
A
B
C
D
E
F
STORE BUFFER
MMU
TLB
HOST ADDRESS
DATA & INSTRUCTIONS
DATA
TARGET ADDRESS
INST. CACHE
DATA IN
INTEGER UNIT
OFFICIAL REGISTERS
WORKING REGISTERS
INSTRUCTION FETCH & DISPATCH
FLOATING POINT UNIT
OFFICIAL REGISTERS
WORKING REGISTERS

FIGURE 3

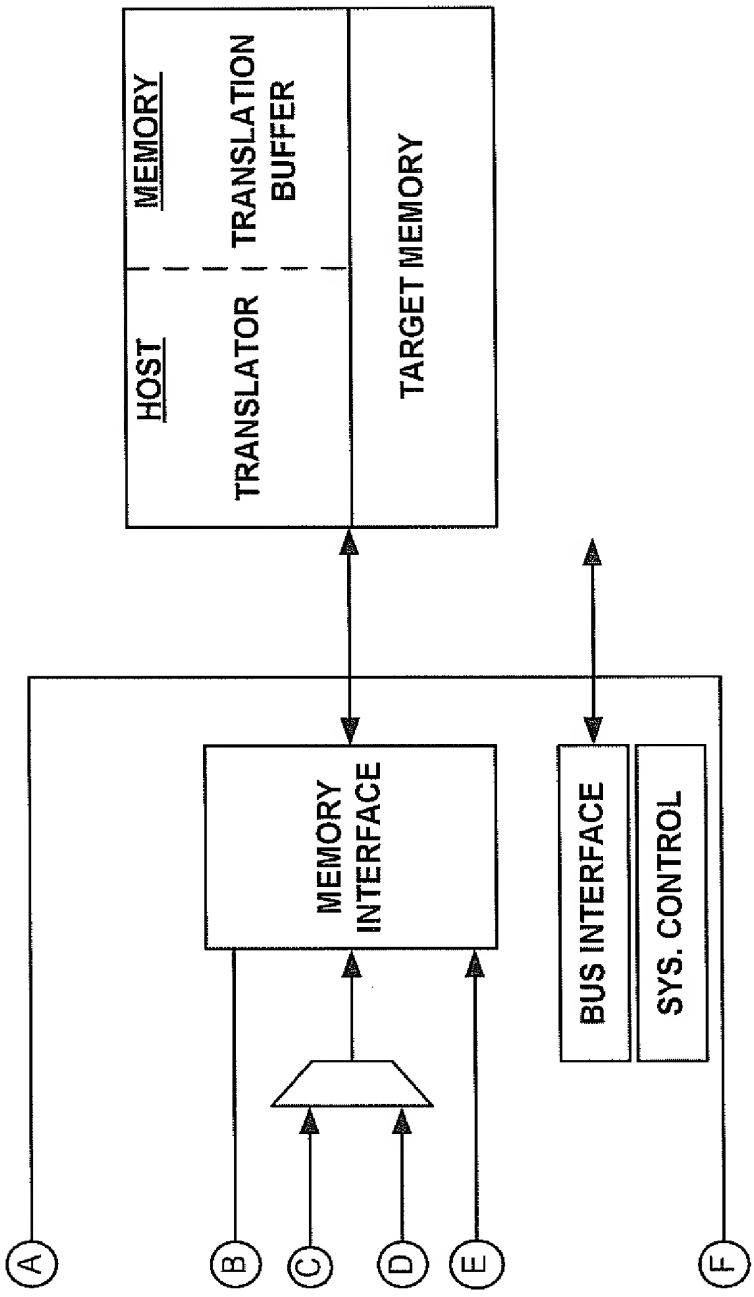

FIGURE 3 (CONT.)

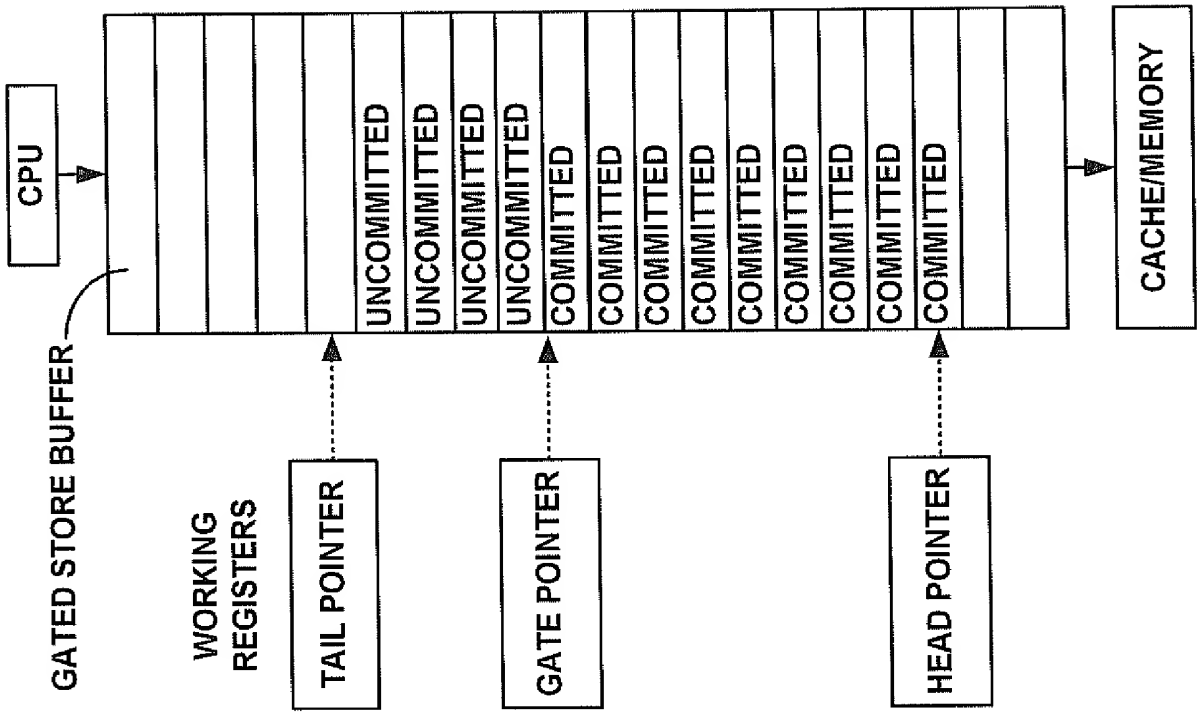

FIGURE 5

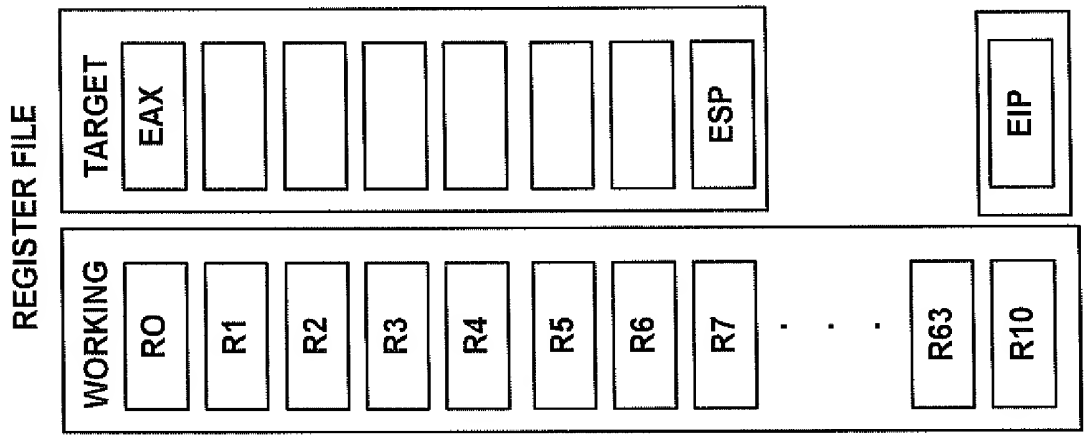

FIGURE 4

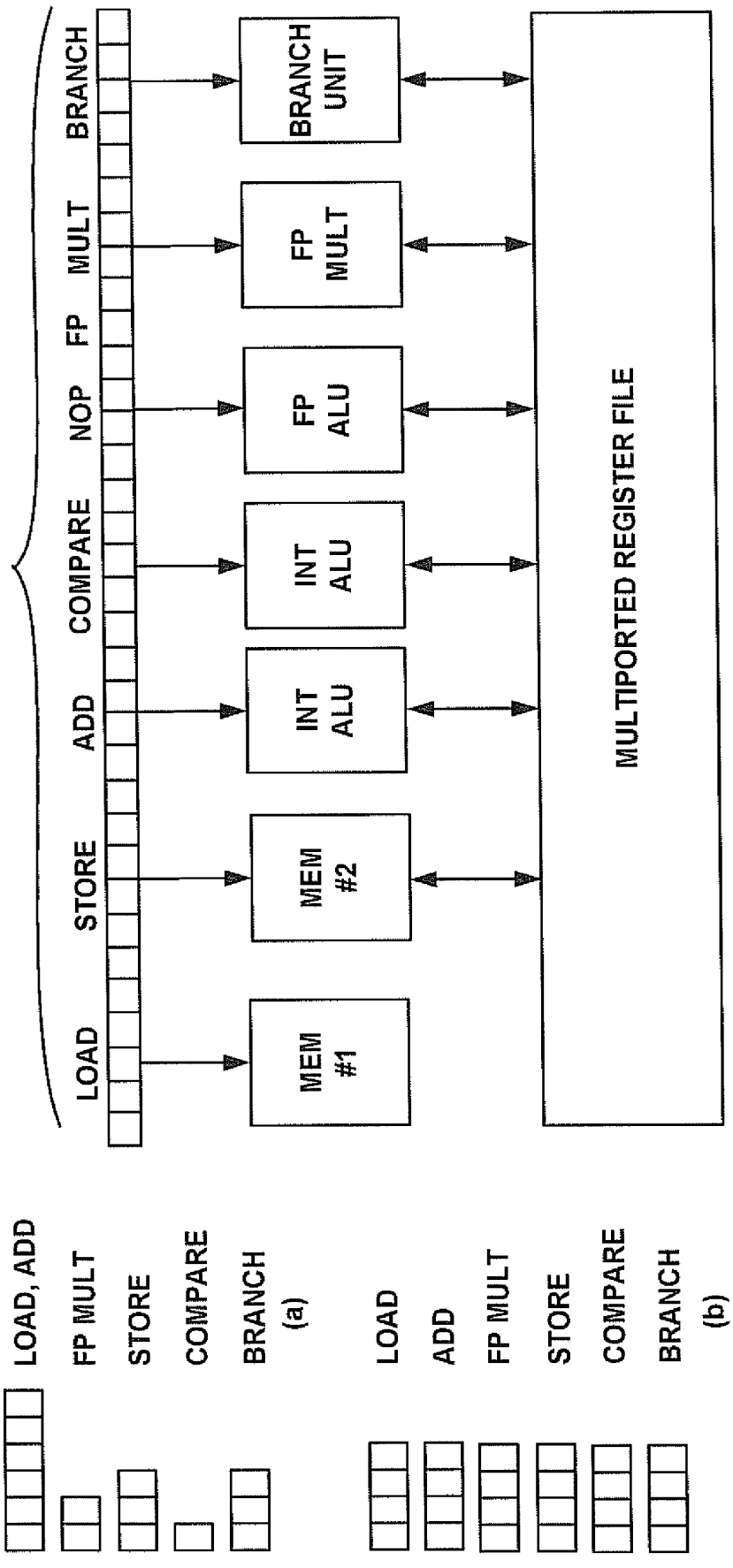
LOAD, ADD
FP MULT
STORE
COMPARE
BRANCH
(a)
LOAD
ADD
FP MULT
STORE
COMPARE
BRANCH
(b)
SINGLE VLIW INSTRUCTION
LOAD
STORE
ADD
COMPARE
NOP
FP
MULT
BRANCH
MEM #1
MEM #2
INT ALU
INT ALU
FP ALU
FP MULT
BRANCH UNIT
MULTIPORTED REGISTER FILE
(c)

FIGURE 6

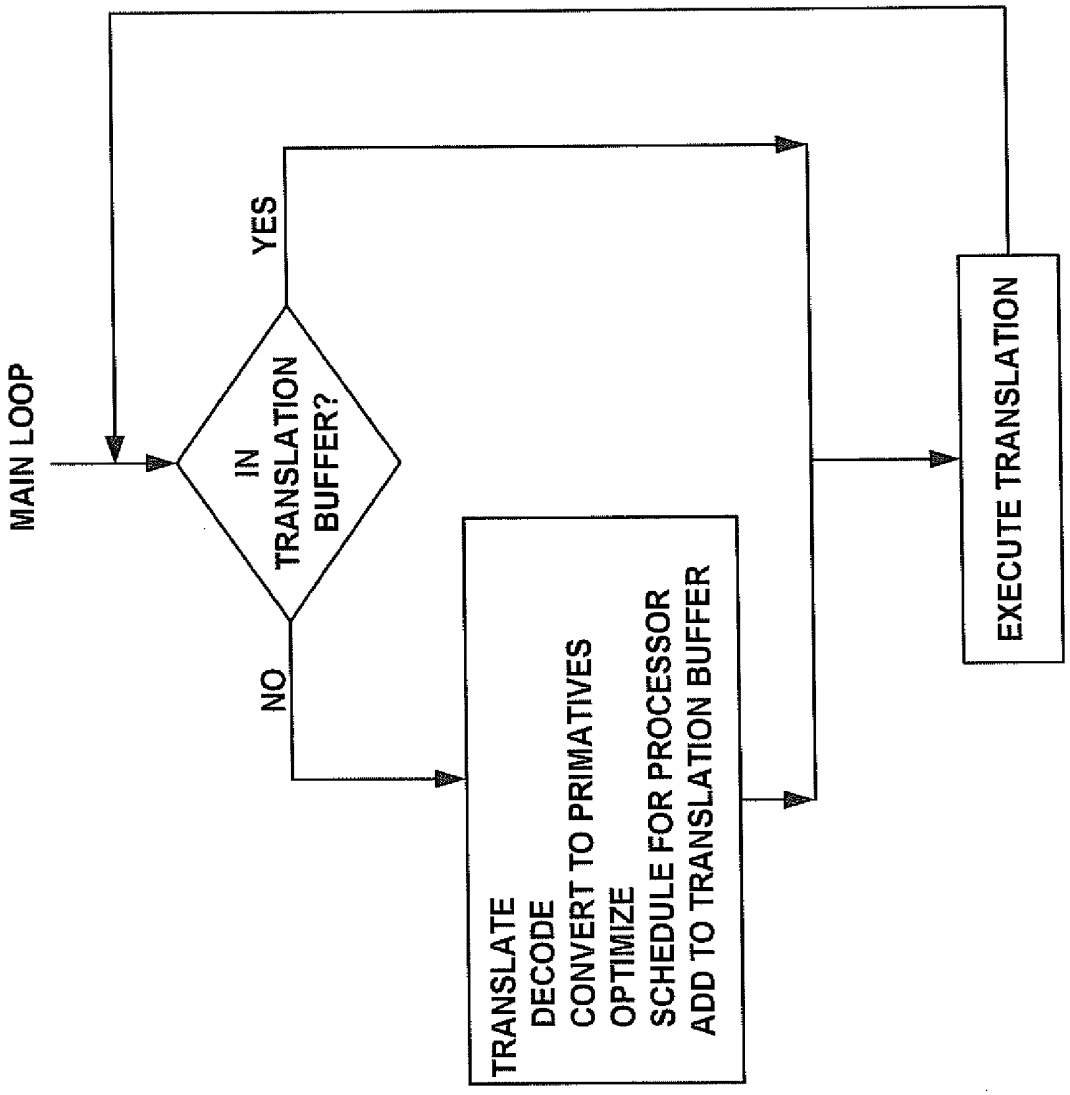
MAIN LOOP
IN TRANSLATION BUFFER?
YES
NO
TRANSLATE
DECODE
CONVERT TO PRIMATIVES
OPTIMIZE
SCHEDULE FOR PROCESSOR
ADD TO TRANSLATION BUFFER
EXECUTE TRANSLATION

FIGURE 7

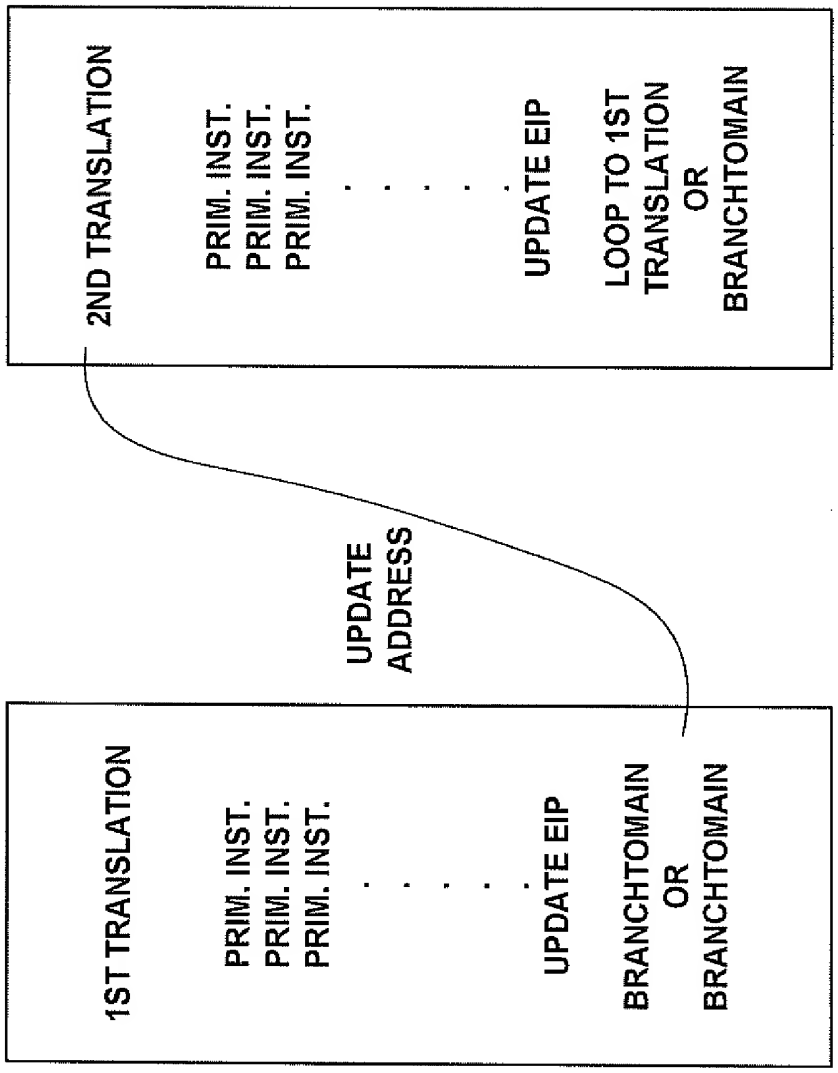
1ST TRANSLATION
PRIM. INST.
PRIM. INST.
PRIM. INST.
UPDATE EIP
BRANCHTOMAIN
OR
BRANCHTOMAIN
UPDATE
ADDRESS
2ND TRANSLATION
PRIM. INST.
PRIM. INST.
PRIM. INST.
UPDATE EIP
LOOP TO 1ST
TRANSLATION
OR
BRANCHTOMAIN

FIGURE 8

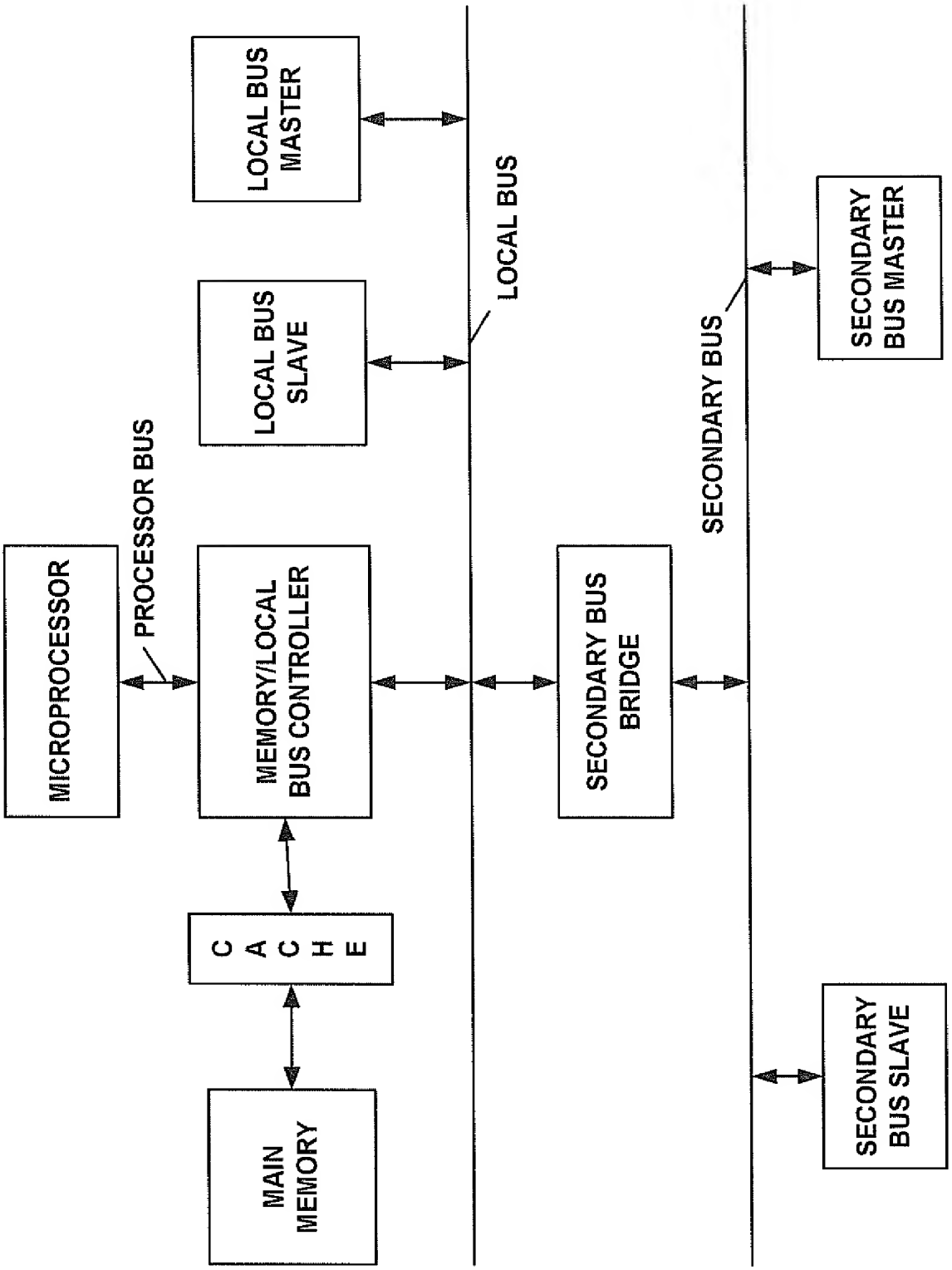
MICROPROCESSOR
PROCESSOR BUS
MEMORY/LOCAL BUS CONTROLLER
C A C H E
MAIN MEMORY
LOCAL BUS MASTER
LOCAL BUS SLAVE
LOCAL BUS
SECONDARY BUS BRIDGE
SECONDARY BUS
SECONDARY BUS MASTER
SECONDARY BUS SLAVE

FIGURE 9

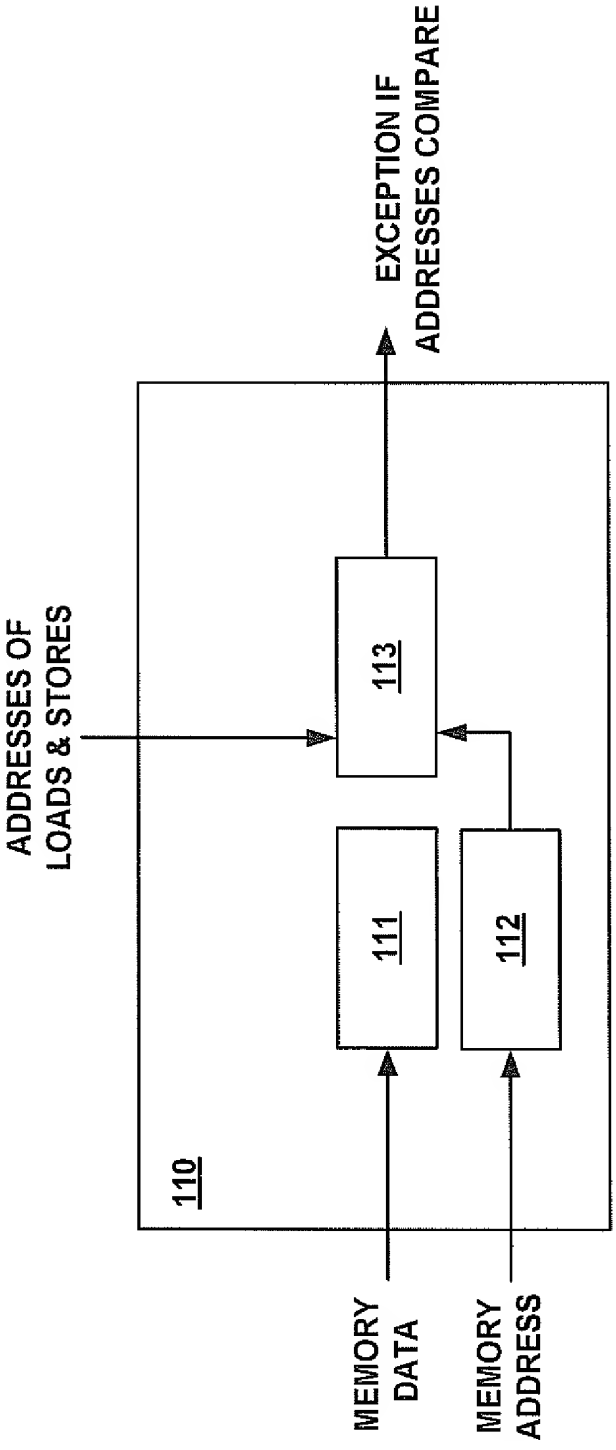
EXCEPTION IF
ADDRESSES COMPARE
ADDRESSES OF
LOADS & STORES
113
111
112
110
MEMORY
DATA
MEMORY
ADDRESS

FIGURE 10

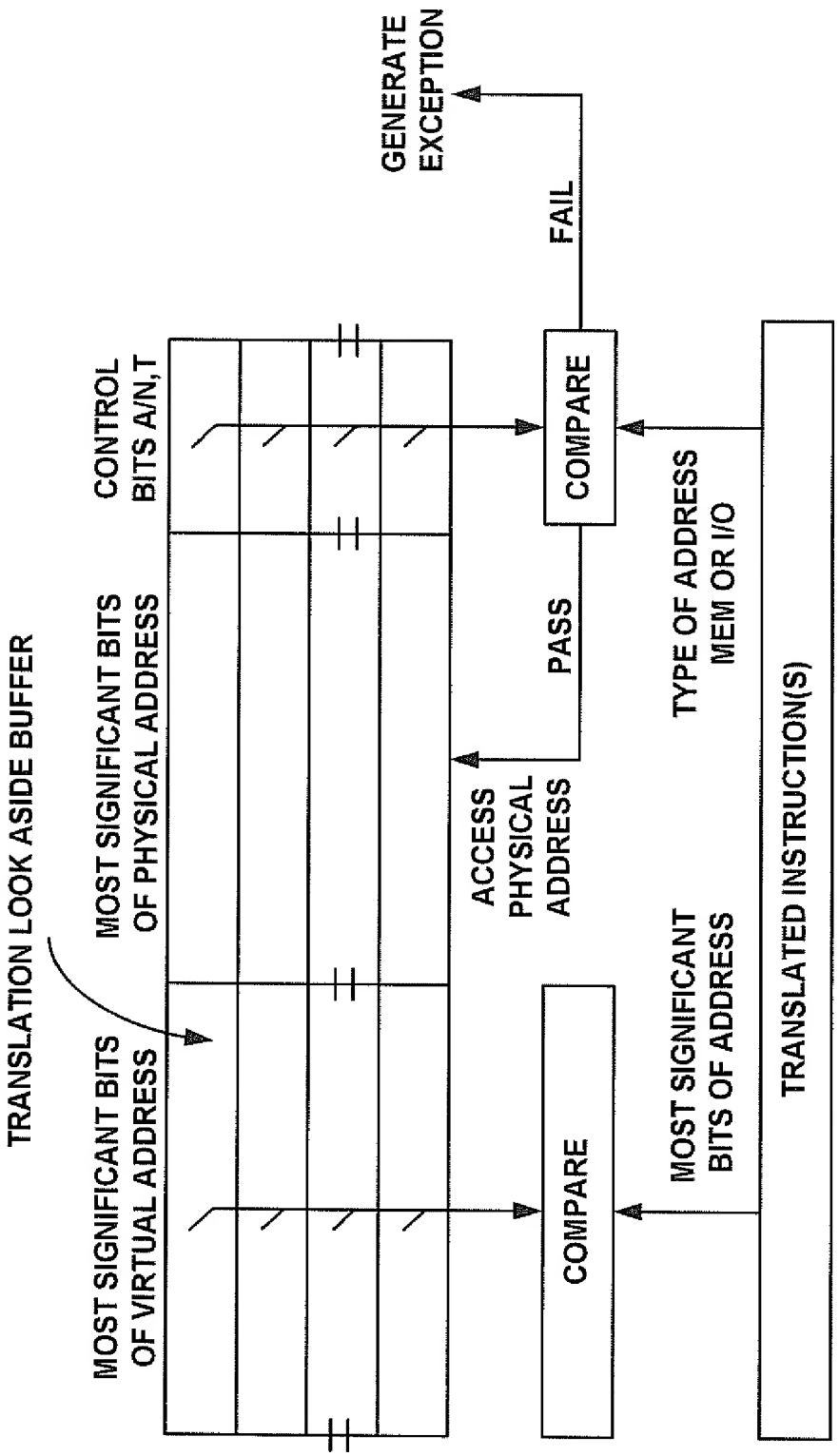
TRANSLATION LOOK ASIDE BUFFER
MOST SIGNIFICANT BITS OF VIRTUAL ADDRESS
MOST SIGNIFICANT BITS OF PHYSICAL ADDRESS
CONTROL BITS A/N,T
COMPARE
COMPARE
ACCESS PHYSICAL ADDRESS
PASS
FAIL
GENERATE EXCEPTION
MOST SIGNIFICANT BITS OF ADDRESS
TYPE OF ADDRESS MEM OR I/O
TRANSLATED INSTRUCTION(S)

FIGURE 11